AMENDMENTS TO THE CLAIMS

Claim 1 (currently amended): A semiconductor memory device, comprising:

a memory array comprising a plurality of memory cells;

a page buffer section for temporarily storing data to be written into the memory array, and wherein data from the page buffer is processed for prohibiting unnecessary data from being written into the plurality of memory cells; and

a masking section for masking at least a portion of data read from the page buffer section based on a characteristic of a particular write operation regarding that data.

Claim 2 (previously presented): A semiconductor memory device according to claim 1, wherein the characteristic is a data bus width in the semiconductor memory device.

Claim 3 (previously presented): A semiconductor memory device according to claim 1, wherein:

the masking section comprises a comparison section for comparing a value of an address of the memory array with a value of at least one of a beginning address and an end address of the memory array, when the data is read from the page buffer section; and

the characteristic is a result of the comparison by the comparison section.

Claim 4 (previously presented): A semiconductor memory device according to claim 1, wherein:

the masking section comprises a matching detection section for determining whether or not an address of the memory array is equal to at least one of a beginning address and an end address of the memory array, when the data is read from the page buffer section; and

the characteristic is a result of the determination by the matching detection section.

Claim 5 (previously presented): A semiconductor memory device according to claim 1, wherein:

the masking section comprises a counter section for counting the number of pieces of data to be written into the memory array; and

the characteristic is a result of the counting by the counter section.

Claim 6 (original): A semiconductor memory device according to claim 1,

wherein the masking section comprises a deactivation section for deactivating a portion of the data read from the page buffer section.

Claim 7 (original): A semiconductor memory device according to claim 1, wherein:

each of the plurality of memory cells is a multi-value memory cell capable of storing at least three values; and

the semiconductor memory device comprises a page mode read section for simultaneously reading some of the plurality of memory cells.